Amendments to the Specification:

Please add the following new paragraphs after paragraph 0015:

[0015a] FIG. 7 is a flowchart to show an example of a method of protecting a processor from voltage surges.

[0015b] FIG. 8 is a flowchart to illustrate an example of an approach to accelerating a current ramp down rate.

Please amend paragraph 0029 as follows:

[0029] One approach to accelerating the current ramp down rate is shown in greater detail at block 78' of FIG. 8. Specifically, [[74]] block 84 provides for receiving a level signal, and block 86 provides for converting the level signal into a pulse signal based on a ramp down current measurement, which can be taken via the sensing resistor, R_s (FIG. 4). The width of the pulse can be determined in other ways as well. A surge inductor is switched into a parallel connection with an output inductor of the power output stage at block 88 in order to reduce the effective inductance of the ramp down current path of the power output stage. This phenomenon is shown further in the plot 92 of FIG. 6 in which a conventional current ramp down curve 94 is compared to an accelerated current ramp down curve 96. As can be seen in FIG. 6, the new inductor current ramp down rate is much faster than that of the old inductor current plot. Due to the faster discharge rate, the output voltage surge is significantly reduced. As such, the output voltage stays within the allowable tolerance window or V_{MAX}.